

Model  
H-264



Owner's Manual



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# User Agreement/ WATERLOG® Warranty

## **1. NATURE OF THE PRODUCT**

This agreement accompanies a pressure measuring/data collection system comprising micro-coded circuitry and other electronic equipment sealed in an enclosed housing and packaged together with written instructional materials. The packaged electronic circuitry and instructional materials herein are collectively referred to as the "PRODUCT." The PRODUCT is made available from DESIGN ANALYSIS ASSOCIATES, INC., of 75 West 100 South, Logan, Utah 84321 (hereinafter referred to as "DESIGN ANALYSIS"), and contains information and embodies technology that is confidential and proprietary to DESIGN ANALYSIS, and the availability and use of the PRODUCT is extended to you, the USER, solely on the basis of the terms of agreement which follow.

## **2. ACKNOWLEDGMENTS BY USER**

Opening the package which encloses the accompanying PRODUCT indicates your acceptance of the terms and conditions of this agreement and constitutes an acknowledgment by you of the confidential and proprietary nature of the rights of DESIGN ANALYSIS in the PRODUCT.

## **3. DUTIES OF YOU, THE USER**

In consideration for the access to and use of the PRODUCT extended to you by DESIGN ANALYSIS, and to protect the confidential and proprietary information of DESIGN ANALYSIS, USER agrees as follows:

- (a) USER agrees that they will not open the sealed housing of the PRODUCT, and that they will take all necessary precautions to prevent their employees, agents, subcontractors, and resellers from doing so.
- (b) USER agrees that they will not remove from the exterior of the housing of the PRODUCT any warnings against opening or notices of proprietary interest placed thereon by DESIGN ANALYSIS, and that they will take all necessary precautions to prevent their employees, agents, subcontractors, and resellers from removing such markings therefrom.
- (c) USER agrees to treat the PRODUCT with the same degree of care as USER exercises in relation to their own confidential and proprietary information.
- (d) USER agrees to return the PRODUCT to DESIGN ANALYSIS if and when the PRODUCT is deemed to be no longer of use. In return therefore, USER will receive from DESIGN ANALYSIS a redemption fee of \$10.00.

#### **4. TERM**

USER may enjoy these rights only as long as their possession of the PRODUCT shall continue to be rightful. These rights will cease if the PRODUCT is returned to DESIGN ANALYSIS under the terms of any redemption offer, warranty, or money-back guarantee, or if USER transfers the PRODUCT to another party on terms inconsistent with this agreement.

#### **5. LIMITED WARRANTY**

##### **(a) What is Covered**

DESIGN ANALYSIS warrants that for a period of twelve months from the time of purchase the functions to be performed by the PRODUCT will be substantially in compliance with USER documentation. DESIGN ANALYSIS also warrants that the PRODUCT will be free from defects in materials and workmanship for a period of ONE YEAR from the date of purchase.

##### **(b) What USER Must Do**

If the product fails to satisfy the above warranty, USER must notify DESIGN ANALYSIS in writing within the applicable period specified above, and reasonably cooperate with the directions they receive from DESIGN ANALYSIS.

##### **(c) What DESIGN ANALYSIS Will Do**

DESIGN ANALYSIS will repair the PRODUCT, or will endeavor to provide a replacement of same within a reasonable period of time. In the event that DESIGN ANALYSIS is unable to make the necessary repairs or replacement within a reasonable period of time, the original purchase price will be refunded upon the return of the PRODUCT to DESIGN ANALYSIS.

##### **(d) Limitations**

- (i) THIS LIMITED WARRANTY IS VOIDED WHERE THE SEALED HOUSING OF THE PRODUCT HAS BEEN OPENED.**
- (ii) THE ENTIRE REMEDY FOR BREACH OF THIS LIMITED WARRANTY SHALL BE LIMITED TO REPLACEMENT OF THE DEFECTIVE PRODUCT OR REFUNDING OF THE PURCHASE PRICE, AS SET FORTH ABOVE. IN NO EVENT WILL THE LIABILITY OF DESIGN ANALYSIS TO USER OR TO ANY OTHER PARTY EXCEED THE ORIGINAL PURCHASE PRICE OF THE PRODUCT, REGARDLESS OF THE FORM OF THE CLAIM.**

- (iii) EXCEPT FOR THE EXPRESS WARRANTIES ABOVE, DESIGN ANALYSIS SPECIFICALLY DISCLAIMS ALL OTHER WARRANTIES, INCLUDING, WITHOUT LIMITATION, ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.
- (iv) UNDER NO CIRCUMSTANCES WILL DESIGN ANALYSIS BE LIABLE FOR SPECIAL, INCIDENTAL, CONSEQUENTIAL, INDIRECT, OR ANY OTHER DAMAGES OR CLAIMS ARISING FROM THE USE OF THIS PRODUCT, THIS INCLUDES LOSS OF PROFITS OR ANY OTHER COMMERCIAL DAMAGES, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. IN NO EVENT WILL DESIGN ANALYSIS BE LIABLE FOR ANY CLAIMS, LIABILITY, OR DAMAGES ARISING FROM MODIFICATION MADE THEREIN, OTHER THAN BY DESIGN ANALYSIS.
- (v) Should the exclusive remedy stated in subparagraph 6 (d) (ii) above be determined by a proper court of law to have failed of its essential purpose, the limitation of the obligations of DESIGN ANALYSIS stated in subparagraphs 6 (d) (iii) and (iv) shall remain valid.
- (vi) THIS LIMITED WARRANTY GIVES USER SPECIFIC LEGAL RIGHTS. USER MAY ALSO HAVE OTHER RIGHTS WHICH VARY FROM STATE TO STATE. SOME STATES DO NOT ALLOW LIMITATIONS ON HOW LONG AN IMPLIED WARRANTY LASTS OR THE EXCLUSION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES, SO THOSE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY.

## **6. BINDING AGREEMENT**

This is a binding agreement, and if not understood, USER should seek competent legal advice. By paying for the PRODUCT and opening the package, USER acknowledges to have read this Agreement and has agreed to be bound by its terms and conditions.

## **7. GOVERNING LAW**

This Agreement and its validity and interpretation shall be governed by the laws of the State of Utah, notwithstanding any choice of law rules of Utah or any other state or jurisdiction.

## **8. U.S. GOVERNMENT RESTRICTED RIGHTS**

Use, duplication, or disclosure by the United States Government is subject to restrictions set forth in paragraph (c) (1) (ii) of the rights in Technical Data and Computer Software clause at 52.227-7013. The Contractor-manufacturer is DESIGN ANALYSIS ASSOCIATES, INC., 75 West 100 South, Logan, Utah 84321.



## ALERT Serial Interface (ASI)

### Overview

The ALERT Serial Interface (ASI) is a multi-purpose device that accepts ALERT ID and data reports in variety of serial data formats. It buffers, parses, and converts them to 300 baud FSK audio signals in binary ALERT format. The device controls power, audio and PTT lines of an attached transmitter to send a standard ALERT binary format transmission.

### Outputs

The ASI transmitter interface is 4 wire, consisting of Switched Battery Power, "Push to Talk" (PTT), Ground and FSK Audio. The FSK Audio signal is an AC coupled, 200mV, low distortion sine wave signal suitable for commonly used ALERT RF transmitters, such as Maxon. The audio level is set with a resistive divider allowing a selection during manufacturing for a maximum of 707mV RMS FSK Audio for transmitters requiring a different audio level input. The ASI switches up to 3 Amp of nominal 12V battery power to the transmitter with typically less than 0.05 V drop at 1 A. The PTT transmitter control output is an NPN open collector.

### Serial Inputs

The serial data input interface type, baud rate and message format selection is with 5 (out of an 8 bit) DIP switches. Although various formats are supported, only one format is selectable at one time. The following signaling modes are supported:

- **Asynchronous RS232:** Data values are received from a standard RS232 serial port at 300, 1200 or 4800 baud using 8 bit data, no parity, one start bit and one stop bit, with no hardware or software handshaking. The interface is a 2 wire interface, using a data and a signal ground. The interface levels meet the EIA RS232 specifications, (i.e. MARK is a maximum of -3 volts, and SPACE is a minimum of +3 V).
- **Asynchronous Logic Levels:** This mode differs only in the interface levels from the RS-232, where nominal Logic Level signals are used in place of RS232. Signaling is conventional (positive logic): 0 V (gnd) is SPACE (bit value 0) and greater than +3 volts is MARK (bit value 1). The interface is design to accommodate signals from 3 or 5 volt logic systems, but can be used for nominal 12 volt systems also.
- **Synchronous Logic Levels:** The electrical interface levels are Logic Levels (as above). A clock (or strobe) signal is controlled by the sending device. Each positive clock transition clocks the bit value on the data line at that time into the ASI. No start or stop bits are used. The maximum clock rate is 500 Hz (2 milliseconds/bit) and the minimum clock rate is 33 Hz (30 milliseconds/bit). Minimum clock pulse width, positive or negative, is 1 millisecond, but otherwise there is no specification on clock duty cycle.

The following two serial input data formats are supported:

- **Binary message values:** A message consists of four bytes. The first two bytes comprise the ID value as a binary integer between 0 and 8191. The second two represent the data value as a binary integer between 0 and 2047. This format is used with asynchronous (RS232 or Logic Level) and synchronous logic level signaling. Synchronous logic level signaling requires the binary information be sent ID value first, followed by the data value, sent as two 16 bit words, sent least significant bit first. Asynchronous signaling requires the binary information be sent as 2 bytes of ID value first, followed by 2 bytes of data value, each sent least significant 8 bit byte first, followed by the most significant byte.
- **ASCII message values:** Each message consists of 8 ASCII characters. The first four represent the ID and the second four represent the data value. Within each 4 character number the byte ordering is most significant character first and least significant character last. All ASCII values other than those representing the digits 0 through 9 are ignored. This format can only be enabled with asynchronous (RS232 or Logic Level) signaling.

## Processing

The ASI typically runs in a low power “idle” mode awaiting serial input. Input buffering is activated at the first bit received (synchronous signaling) or first byte received (asynchronous signaling). Data is buffered continuously until a pause of 100 milliseconds (+/- 20 milliseconds) occurs in the serial input stream. (If the input buffer is filled prior to a 100 milliseconds pause, an “overrun” is flagged. When the next pause does occur, the ASI processes and transmits the maximum ALERT messages allowed factory set in software at 10 messages, beginning with the “first-in” message.)

After any 100 milliseconds pause on the serial input, the contents of the input buffer are parsed according to rules specific to the input format into 16 bit words. Each pair of 16 bit words is considered a 16 bit ID value followed by a 16 bit data value and converted into an ALERT 4-byte binary format message (40 bits). Each ID value is not checked to be less than 8192, but is converted to a value less than 8192. Similarly, each data value is not checked to be less than 2048, but is converted to a value less than 2048. Parsing of pairs of 16 bit words continues until all pairs in the buffer are converted, or a maximum of 10 ALERT messages are formed. Any remaining 16 bit words are discarded.

After the maximum number of ALERT messages are processed (10), all messages are transmitted in a single RF transmission. When more than one ALERT message is transmitted, an inter-message delay (MARK tone) of 40 milliseconds is inserted preceding each message subsequent to the first.

Transmission preamble length is selectable from 101 milliseconds to 665 milliseconds, in increments of 81.5 milliseconds, with 3 (from an 8 bit) DIP switch. The transmission preamble is evenly divided between the initial clear carrier (no modulation) and MARK tone modulation. For example, with a 101 milliseconds preamble selected, the transmitter is keyed (PTT turned on) for 50.5 milliseconds with no audio input, followed by 50.5 milliseconds of MARK tone audio, followed by a message of 40 FSK encoded binary bits at 300 bits/sec and, if multiple messages are being transmitted, repeatably followed by a 40 millisecond MARK tone delay and another message. The transmitter “warm-up” time (time between “Switched Battery Power” turned on at transmitter connector until the assertion of PTT) is factory set to 100 milliseconds.

A duty cycle timer enforces a 12 second (factory set in software) delay between transmissions. A hardware watch-dog timer is used during transmissions to enforce a maximum transmitter on time to less than 1 second for a single message transmission and less than 3.25 seconds for multiple message transmissions.

The ASI serial input is double buffered. Immediately following a serial input pause and until the completion of the processing and transmission of the serial input message(s) received before the pause, a second buffer is used to accumulate serial data input. During this time period, all serial input is buffered into the second buffer regardless of any serial input pauses, (i.e. the serial messages are concatenated).

Following the completion of the ALERT transmission, if serial input has been buffered, the ASI again waits for a 100 milliseconds pause on the serial input, after which that buffer contents is processed. Immediately following a serial input pause and until the completion of the processing, *duty cycle wait time expiration* and transmission of this serial input message(s), the first buffer is used again to accumulate serial data input. During this time period (including the *12 second duty cycle wait time*), all serial input is buffered into a single buffer regardless of any serial input pauses, (i.e. the serial messages are concatenated).

If fatal errors occur during serial input, data processing or transmission, the ASI jumps to its error processing routine. Error processing consists of ensuring the transmitter is off, waiting 30 seconds (+/- 6 seconds), and then performing a software reset (which re-initializes all I/O and buffers.) During the reset process all serial input is ignored, and any previous serial input is

discarded. Potential fatal error conditions include: battery voltage falling below the battery voltage cutoff threshold just prior to or during transmission; or internal software error conditions.

## Test Input

A switch input is available which causes a test transmission. On switch contact opening, a single ALERT message is transmitted, with a factory set ID value of 5000 and a data value which increments on each on each contact "break". This test input is not buffered, and multiple occurrences during a transmission and duty cycle wait period are treat as a single "break" occurrence. Note - during a test input transmission only a single serial input buffer is in available to buffer any incoming serial data.

## Power, mechanical

The ASI is designed for a 12V battery/solar power supply. The minimum supply voltage for the ASI board alone is only 4 volts, but most transmitters require a minimum of 9 volts. The ASI board maximum input voltage is 20 volts, but commonly, transmitters have an 18 volt maximum input voltage specification. (The ASI printer circuit board is designed to optionally allow a transmitter to be powered from a separate battery/supply from the ASI itself: contact the factory for assistance in configuring the ASI for split supplies.)

The ASI monitors the battery voltage by averaging eight 315 microsecond analog to digital converter samples of the battery voltage prior to turning on the transmitter, and every 2.5 milliseconds during transmission. If the battery voltage falls below the minimum transmitter battery voltage cutoff, the transmitter is turned off and the error processing state is entered. The threshold is factory set at 9.00 volts (8.92 to 9.08 volts over temperature).

A green LED indicates that the Switched+12 volt supply is turned on, and a red LED indicates that PTT is on.

Typical current consumption is 9 microamps waiting for serial input. During message parsing and processing, typical current consumption is 323 microamps. During high speed processing (ADC operation, digital FSK tone generation) the current consumption is typically 2.8 milliamps, and with the Switched+12 volt LED on, the PTT LED on, and the 3<sup>rd</sup> order audio filter on, the typical current consumption is 10 milliamps.

The ASI is 10.0 cm x 6.20 cm. There are four (0.381 cm diameter) mounting holes. All 4 located 0.40 cm on center from the long top and bottom edges; 2 are located 0.4 cm on center from the right narrow edge and the other 2 are located 2.0 cm on center from the left narrow edge.

The 2 pin input battery and 4 pin transmitter screw terminal connectors are located along the left narrow edge. The 4 pin serial input screw terminal connector, 2 pin test input header and 4 pin AuxRS232 header are located along the right narrow edge.

## Operational Mode, DIP Switch Selection Settings

For changes in DIP switch settings to be effective, the ASI must be RESET after new switch settings are entered. A RESET is done by either depressing the RESET switch on the ASI board for 5 seconds or by powering the ASI board off for at least 90 seconds.

### ***Baud Rate & ASYNC/SYNC selection***

Switch 1		Switch 2		
Open	0	Open	0	ASYNC (LL or RS232) 300 Baud
Closed	1	Open	0	ASYNC (LL or RS232) 1200 Baud
Open	0	Closed	1	ASYNC (LL or RS232) 4800 Baud
Closed	1	Closed	1	SYNC SERIAL (LL SCLK & LL DATA Input only)

### ***Incoming Message Format***

Switch 3		Switch 4		
Open	0	Open	0	ALERT binary format (16 bits ID, 16 bits Data)
Closed	1	Open	0	ALERT ASCII format (4 chars ID, 4 chars Data)
Open	0	Closed	1	Reserved - Do not use
Closed	1	Closed	1	Diagnostic Mode if S1 & S2 are 1 (see Diagnostic Mode DIP switch settings), otherwise Reserved – Do not use.

### ***ALERT Transmission Preamble Length (1/2 clear carrier, 1/2 mark tone)***

Switch 5		Switch 6		Switch 7		
Open	0	Open	0	Open	0	101 milliseconds
Closed	1	Open	0	Open	0	182
Open	0	Closed	1	Open	0	262
Closed	1	Closed	1	Open	0	343
Open	0	Open	0	Closed	1	424
Closed	1	Open	0	Closed	1	504
Open	0	Closed	1	Closed	1	585
Closed	1	Closed	1	Closed	1	665

### ***ASYNC Input Voltage level Selection***

***(Note – this switch has no effect if SYNC serial is enable with Switch 1 & Switch 2)***

Switch 8		
Open	0	Logic Level input selected (0 V = 0, 3 to 5 V = 1)
Closed	1	RS232 (EIA) levels

**Operational Mode Selection Matrix**

The matrix below shows all the Operational Modes and their corresponding DIP Switch settings (but without expanding the 3 Transmission Preamble Length switch settings). In the matrix “x” means “don’t care” and “p” means preamble length time setting switch input.

S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	Async or Sync & Baud Rate	Incoming Message Format	Preamble Length (msec)	RS232 or Logic Level Input
0	0	0	0	p	p	p	0	Async, 300	Binary	S5,S6,S7	Logic Levels
1	0	0	0	p	p	p	0	Async, 1200	Binary	S5,S6,S7	Logic Levels
0	1	0	0	p	p	p	0	Async, 4800	Binary	S5,S6,S7	Logic Levels
1	1	0	0	p	p	p	0	Sync	Binary	S5,S6,S7	Logic Levels
0	0	1	0	p	p	p	0	Async, 300	ASCII	S5,S6,S7	Logic Levels
1	0	1	0	p	p	p	0	Async, 1200	ASCII	S5,S6,S7	Logic Levels
0	1	1	0	p	p	p	0	Async, 4800	ASCII	S5,S6,S7	Logic Levels
1	1	1	0	p	p	p	0	Sync	ASCII	S5,S6,S7	Logic Levels
x	x	0	1	x	x	x	x		Reserved		
0	0	1	1	x	x	x	x		Reserved		
1	0	1	1	x	x	x	x		Reserved		
0	1	1	1	x	x	x	x		Reserved		
1	1	1	1	x	x	x	x		Diagnostic		
0	0	0	0	p	p	p	1	Async, 300	Binary	S5,S6,S7	RS232 Levels
1	0	0	0	p	p	p	1	Async, 1200	Binary	S5,S6,S7	RS232 Levels
0	1	0	0	p	p	p	1	Async, 4800	Binary	S5,S6,S7	RS232 Levels
1	1	0	0	p	p	p	1	Sync	Binary	S5,S6,S7	Logic Levels
0	0	1	0	p	p	p	1	Async, 300	ASCII	S5,S6,S7	RS232 Levels
1	0	1	0	p	p	p	1	Async, 1200	ASCII	S5,S6,S7	RS232 Levels
0	1	1	0	p	p	p	1	Async, 4800	ASCII	S5,S6,S7	RS232 Levels
1	1	1	0	p	p	p	1	Sync	ASCII	S5,S6,S7	Logic Levels
x	x	0	1	x	x	x	x		Reserved		
0	0	1	1	x	x	x	x		Reserved		
1	0	1	1	x	x	x	x		Reserved		
0	1	1	1	x	x	x	x		Reserved		
1	1	1	1	x	x	x	x		Diagnostic		

**Diagnostic Mode, Production & Field Testing, DIP Switch Selection Settings**

CAUTION – the diagnostic tests are designed to be run WITHOUT any transmitter connected to the ASI board. Although all tests are designed so as not to turn the “PTT” and “SW+12” line on simultaneously, it may be possible to damage a transmitter (or ASI board) if some of the Diagnostic Mode Tests are entered with a transmitter attached. It is prudent to disconnect any transmitter prior to running diagnostic tests.

Remember that for changes in DIP switch settings to be effective the ASI must be RESET after new switch settings are entered. A RESET is done by either depressing the RESET switch on the ASI board for 5 seconds or by powering the ASI board off for at least 90 seconds.

Once a diagnostic routine is begun, it runs continuously (unless an internal error occurs). In order to exit a diagnostic test and enter a different test, or to return to an operational mode, the ASI board must be RESET. A RESET is done by either depressing the RESET switch on the ASI board for 5 seconds or by powering the ASI board off for at least 90 seconds.

The diagnostic test routines are explained in detailed below.

S1	S2	S3	S4	S5	S6	S7	S8	
1	1	1	1	0	0	0	0	Field Test Tool
1	1	1	1	1	0	0	0	Generate 1000 Hz on Tone Out (SW+12 on, PTT off)
1	1	1	1	0	1	0	0	Generate 1920 Hz on Tone Out (SW+12 on, PTT off)
1	1	1	1	1	1	0	0	Generate 2140 Hz on Tone Out (SW+12 on, PTT off)
1	1	1	1	0	0	1	0	Generate 4062.5 Hz on Tone Out (SW+12 on, PTT off)
1	1	1	1	1	0	1	0	Turn on PTT LED when BatVoltage Avg < VBatCutoff
1	1	1	1	0	1	1	0	Toggle PTT LED at Short SW Delay (about 20 msec) rate
1	1	1	1	1	1	1	0	Toggle PTT LED at Long SW Delay (about 30 sec) rate
1	1	1	1	0	0	0	1	Load test control: toggle SW+12 at 30 sec rate
1	1	1	1	1	0	0	1	DIP Switch Test, send DIP switch out RS232 @ 1200 baud
1	1	1	1	0	1	0	1	BatVoltage Avg out RS232 @ 1200baud & PTT on < VBatCutoff
1	1	1	1	0	1	1	1	Put High Speed Xtal MCLK on P16 & Xtal2 on ACLK
1	1	1	1	1	1	1	1	Put DCO MCLK on P16
1	1	1	1	x	x	x	x	Any other: put DCO MCLK on P16

**Field Test Tool**

In this mode, the ASI can be used to assist in field transmission path analysis. The ASI requires no input. It transmits an ALERT binary message about every 20 seconds, (20.00 seconds from the end of one transmission to the start of the next transmission). The ASI uses an ID of 5000 and the transmitted data value increments on every transmission, initially starting at value 0 on RESET.

**Production Test Routines**

**Generate Tone Out (4 separate diagnostic routines)**

This diagnostic checks the FSK generation code, high frequency oscillator and the 3<sup>rd</sup> order lowpass filter transfer response. The processor powers on the filter, enables the tone output and generates a continuous frequency. To accurately measure the frequency use the square wave output test point “DTone” test point (P14); all frequency measurements should be within +/- 0.5 Hz, when measured at room temperature. To measure the filter transfer response, examine the signal at the analog filter output “ToneOut” test point (P14). With the 1920 & 2140 Hz the analog signal should approximate a sine wave at 200mV RMS centered at ½ the supply voltage (3.3V/2 or approximately 1.65 V); at 4062.5 Hz the signal should be less than 80 mV RMS. At 1000 Hz, the signal shape will not be a sine wave and but more like a contorted square wave, yet still should measure approximately 200mV RMS. The tolerance on these RMS levels is +/- 10%. During these tests the transmitter “Switched Battery Power” is turned on (required to power the filter circuit) which unintentionally powers any transmitter connected, but the transmitter “PTT” is not asserted during the test.

**Turn on PTT LED when BatVoltage Avg < VBat Cutoff**

This diagnostic checks the battery voltage monitor resistive divider network, the 12 bit Analog to Digital Converter (ADC) and the ADC reference circuit. The battery monitor circuit is enabled and the ADC continuously measures and calculates an 8 sample average of the input battery voltage. If the average drops below the minimum transmitter battery voltage threshold (set for 9.00 volts), the PTT LED is turned on. As designed, with a 0.5%, 50 ppm/degC reference and 0.1% resistors in the battery voltage monitor network, the worst case error (over the full operating temperature range, excluding ADC non-linearity) is +/- 0.85%. The PTT LED illumination range is therefore 8.92 V to 9.08 V. During the test, the transmitter “Switched Battery Power” is not turned on, and since the PTT transmitter interface is an open collector, normally this test may be performed with a transmitter connected.

***Toggle PTT LED at Short Software Delay rate (SWDelayS)***

This diagnostic checks that the intrinsic RC DCO frequency of the MSP430 is within nominal tolerance. The DCO clock is as the microprocessor's main clock during serial input parsing and conversion, used to time the 100 millisecond "serial input pause" and the 30 second delay in the error handling routine prior to calling a software reset. None of these processes or timing requires a particularly precise time base, so the DCO clock is used. During the diagnostic, the processor toggles the PTT LED approximately every 20 milliseconds, for a frequency of 25 Hz at the "PTT" test point (P23). At room temperature the tolerance is +/- 20%. During the test, the transmitter "Switched Battery Power" is not turned on, and since the PTT transmitter interface is an open collector, normally this test may be performed with a transmitter connected.

***Toggle PTT LED at Long Software Delay rate (SWDelayL)***

This diagnostic is a duplicate of the "Short Software Delay rate" routine except a longer software delay timer is used, having a toggle rate of approximately 30 seconds. Again the tolerance is +/- 20% at room temperature. This delay routine is used operationally only to generate the wait time before calling a software reset in the error handler. During the test, the transmitter "Switched Battery Power" is not turned on, and since the PTT transmitter interface is an open collector, normally this test may be performed with a transmitter connected. (The next diagnostic routine, the "Load test control", also uses this software delay timer.)

***Load test control: toggle SW+12 at 30 sec rate***

This diagnostic is designed to be used in conjunction with an external load resistor (a 5.0 ohm, at least 25 W, power resistor) to measure the voltage drop and calculate the internal resistance of the transmitter "Switched Battery Power" power MOSFET during a high load. The processor turns the "Switched Battery Power" on for approximately 30 seconds, then off for 30 seconds. Using a battery (or high current power supply) set for approximately 12 V, measure the voltage drop between the battery input (pin 2, P10) and the transmitter "Switched Battery Power" (pin 5, P15) during the "Switch Battery Power" ON period. Also measure the battery input voltage during the ON period. Using the measured value of the load resistor, calculate the load current (nominally 2.4 A). Then using the measured voltage drop, calculate the MOSFET resistance during load (R<sub>dson</sub>). It should be less than 0.035 ohms. After confirming the MOSFET resistance is within specification, carefully touch Q2 and confirm it is not warm to the touch. CAUTION – the 5 ohm resistor load is approximately 30 W, so depending on the type power resistor used, it could become very hot, even with the 50% duty cycle. DO NOT LEAVE THIS TEST ON UNATTENDED or ON FOR MORE THAN A FEW MINUTES.

***DIP Switch Test, send DIP switch out RS232 @ 1200 baud***

This diagnostic is used to check that all the DIP switch positions are functional, both in the "open" and "closed" positions. (Obviously, in order to run this test, the DIP switch must be at least partially functional.) It also checks the processor UART0 transmission section, the baud rate generator and the RS232 driver IC. During this diagnostic the processor powers on the DIP switch inputs, reads the 8 bit values, forms a 4 digit ASCII hex value (with the first 2 digits always "00"). This value is output asynchronously using the processor UART0 at 1200 baud (8 bits, no parity, 1 stop bit), followed by a CR and LF, using the RS232 auxiliary output (pin 2, J1, "AuxRS232"). The processor then waits ½ a second and repeats the process. To confirm all DIP switch functions, start this diagnostic, attach a PC serial port "ground" and "receive data" to the "AuxRS232" connector pin 4 and pin 2, respectively, start a terminal emulation program using 1200 baud and monitor the received hex value. Start changing the DIP switches: begin with all "open" the output should be "0000"; set switch 1 to "closed", the output should be "0001"; set switch 2 to "closed", the output should be "0003"; continue sequentially setting increasing dip switches to the "closed" position and monitoring the output progression: "0007", "000F", "001F", ... "00FF".

***BatVoltage Avg out RS232 @ 1200baud & PTT on < VBatCutoff***

This diagnostic is identical to the "Turn on PTT LED when BatVoltage Avg < VBat Cutoff" diagnostic except that the processor also outputs the measured battery voltage average, in counts, at 1200 baud (8 bits, no parity, 1 stop bit) on the auxiliary RS232 ASI output (pin2, J1, "AuxRS232"), every time a new average is calculated. The output is a 5 digit decimal number representing the ADC count (0-4095). The conversion to battery voltage is  $N * 0.0044895 = V$ ,

where N is the decimal count and V is battery voltage. The transmitter cutoff threshold is a count of 2005, at 9.00 volts.

***Put High Speed Xtal MCLK on P16 & Xtal2 on ACLK***

This diagnostic is used to measure the accuracy of the precision crystal time base, and the current consumption during high speed processing. The 6.500 MHz crystal is started, selected as the processor clock and output on "MCLK" (P16). This is the time base used for the FSK tone generation and high speed processing during transmission and therefore is required to be precise. The measured frequency at room temperature should be between 6.500325 MHz and 6.499675 MHz (or +/- 50 ppm). Additionally, the 32.768 kHz crystal clock is output to test point "ACLK" (P17, or J3 pin 2). This is used for baud rate timing, the transmitter "watch dog timer", the transmitter duty cycle timer and the Field Test Tool transmission timer. At room temperature "ACLK" should measure between 32,767.34 Hz and 32,768.66 Hz (or +/- 20 ppm).

***Put DCO MCLK on P16***

This diagnostic is used to measure the RC DCO frequency and current during low speed processing ("Buffer Conversion Processing"). The basic MSP430 RC DCO clock is output on "MCLK" (P16). As described in the SWDelayS and SWDelayL diagnostic routines above, this oscillator specification is very wide. The nominal frequency is 780 kHz (at 3.3 V), but can range between 624 kHz and 934 kHz (+/- 20%).

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